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Substitute for form 1449/PTO Modified	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	Application Number	10/766,698
	Confirmation No.:	2084
	Filing Date:	January 28, 2004
	First Named Inventor:	Wallin, et al.
	Art Unit:	2186
	Examiner Name:	Unknown
Sheet 1 of 4	Attorney Docket Number:	5681-62001

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, (page(s), volume-issue number(s), publisher, city and/or country where published.	Check if English Translation is attached
MB	A1	ANANT AGARWAL, JOHN HENNESSY, and MARK HOROWITZ; Cache Performance of Operating System and Multiprogramming Workloads; Transactions on Computer Systems (TOCS); 1988; Vol. 6, No. 4; pps 393 – 431.	☐
MB	A2	ALAN CHARLESWORTH; The Sun Fireplane System Interconnect; 2001 Conference on Supercomputing; 2001; 14 pages; Denver CO, U.S.A.	☐
MB	A3	TIEN-FU CHEN and JEAN-LOUP BAER; A Performance Study of Software and Hardware Data Prefetching Schemes; International Symposium on Computer Architecture; 1994; pps 223 – 232.	☐
MB	A4	FREDRIK DAHLGREN, MICHEL DUBOIS and PER STENSTROM; Sequential Hardware Prefetching in Shared-Memory Multiprocessors; IEEE Transactions on Parallel and Distributed Systems; 1995; Vol. 6 No. 7; pps 733 – 746.	☐
MB	A5	FREDRIK DAHLGREN and PER STENSTROM; Evaluation of Hardware-Based Stride and Sequential Prefetching in Shared-Memory Multiprocessors; IEEE Transactions on Parallel and Distributed Systems; 1996; Vol. 7, No. 4; pps 385 – 398.	☐
MB	A6	MICHEL DUBOIS, JONAS SKEPPSTEDT, LIVIO RICCIULLI, KRISHNAN RAMAMURTHY, and PER STENSTROM; The Detection and Elimination of Useless Misses in Multiprocessors; International Symposium on Computer Architecture; 1993; pps 88 – 97.	☐

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Examiner Signature	Matthew Bradley	Date Considered	9/3/05

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MB	A7	SUSAN J. EGGERS and TOR E. JEREMIASSEN; Eliminating False Sharing. 1991 International Conference on Parallel Processing; 1991; pps 377 – 381.	☐
MB	A8	SUSAN J. EGGERS and RANDY H. KATZ; The Effect of Sharing on the Cache and Bus Performance of Parallel Programs. International Conference on Architectural Support for Programming Languages and Operating Systems; 1989; pps 257 – 270.	☐
MB	A9	FREDRIK DAHLGREN and PER STENSTROM; Performance Evaluation and Cost Analysis of Cache Protocol Extensions for Shared-Memory Multiprocessors; IEEE Transactions on Computers; 1998; Vol. 47, No. 10; pps 1041 – 1055.	☐
MB	A10	M. J. GARZARAN, J. L. BRIZ, P. E. IBANEZ, and V. VINALS; Hardware Prefetching in Bus-Based Multiprocessors: Pattern Characterization and Cost-Effective Hardware; Parallel and Distributed Processing; 2001, pages 345 – 354.	☐
MB	A11	JAMES R. GOODMAN; Using Cache Memory to Reduce Processor-Memory Traffic; In 25 Years of the International Symposia on Computer Architecture (selected papers); 1998; pps 255 – 262.	☐
MB	A12	ANOOP GUPTA and WOLF-DIETRICH WEBER; Cache Invalidation Patterns in Shared-Memory Multiprocessors. IEEE Transactions on Computers; 1992; Vol. 41, No. 7; pps 794 – 810.	☐
MB	A13	MARTIN KARLSSON, KEVIN MOORE, ERIK HAGERSTEN, and DAVID A. WOOD; Memory System Behavior of Java-Based Middleware; Ninth Annual International Symposium on High-Performance Computer Architecture (HPCA-9); 2003; 12 pages.	☐
MB	A14	DAVID M. KOPPELMAN; Neighborhood Prefetching on Multiprocessors Using Instruction History; International Conference on Parallel Architectures and Compilation Techniques; 2000; pps 123 – 132.	☐
MB	A15	SANJEEV KUMAR and CHRISTOPHER WILKERSON; Exploiting Spatial Locality in Data Caches using Spatial Footprints; International Symposium on Computer Architecture; 1998; pps 357 – 368.	☐
MB	A16	PETER S. MAGNUSSON, MAGNUS CHRISTENSSON, JESPER ESKILSON, DANIEL FORSGREN, GUSTAV HALLBERG, JOHAN HOGBERG, FREDRIK LARSSON, ANDREAS MOESTEDT, and BENGT WERNER; Simics: A Full System Simulation Platform; IEEE Computer, 2002; Vol. 35 No. 2; pps 50 – 58.	☐

Examiner Signature	Matthew Bradley	Date Considered	9/30/06

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MB	A17	TODD MOWRY and ANOOP GUPTA; Tolerating Latency Through Software-Controlled Prefetching in Shared-Memory Multiprocessors; Journal of Parallel and Distributed Computing; 1991; Vol. 12, No. 2; pps 87 – 106.	☐
MB	A18	TODD C. MOWRY; Tolerating Latency in Multiprocessors through Compiler-Inserted Prefetching. Transactions on Computer Systems (TOCS); 1998; Vol. 16, No. 1; pps 55 – 92.	☐
MB	A19	STEVEN PRZYBYLSKI; The Performance Impact of Block Sizes and Fetch Strategies; International Symposium on Computer Architecture; 1990; pps 160 – 169.	☐
MB	A20	ANDRE SEZNEC; Decoupled Sectored Caches: conciliating low tag implementation cost and low miss ratio; 21st Annual International Symposium on Computer Architecture; 1994; pps 384 – 393.	☐
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MB	A22	DEAN M. TULLSEN and SUSAN J. EGGERS; Effective Cache Prefetching on Bus-Based Multiprocessors; Transactions on Computer Systems (TOCS); 1995; Vol. 13, No. 1; pps 57 – 88.	☐
MB	A23	DEAN M. TULLSEN and SUSAN J. EGGERS; Limitations of Cache Prefetching on Bus-Based Multiprocessor; 20th Annual International Symposium on Computer Architecture; 1993; pps 278 - 288.	☐
MB	A24	STEVEN CAMERON WOO, MORIYOSHI OHARA, EVAN TORRIE, JASWINDER PAL SINGH, and ANOOP GUPTA; The SPLASH-2 Programs: Characterization and Methodological Considerations; 22nd Annual International Symposium on Computer Architecture; 1995; pps 24 – 36.	☐
MB	A25	ALEXANDER V. VEIDENBAUM, WEIYU TANG, and RAJESH GUPTA; "Adapting Cache Line Size to Application Behavior"; In Proceedings of the 13th International Conference on Supercomputing; 1999; pps 145 – 154.	☐
MB	A26	http://ecperf.theserverside.com/ecperf/; The publication date of this internet web page predates the filing date of the current application.	☐
MB	A27	http://www.spec.org/jAppServer2001/press_release.html; The publication date of this internet web page predates the filing date of the current application.	☐
MB	A28	http://www.spec.org/jbb2000/; The publication date of this internet web page predates the filing date of the current application.	☐
MB	A29	TIEN-FU CHEN and JEAN-LOUP BAER; An Effective On-Chip Preloading Scheme to Reduce Data Access Penalty; In Proceedings of Supercomputing, 1991; pps176 – 186.	

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MB	A30	EDWARD H. GORNISH; Adaptive and Integrated Data Cache Prefecting For Shared-Memory Multiprocessors; PhD thesis, University of Illinois at Urbana-Champaign; 1995; pps1-150	☐
MB	A31	ERIK HAGERSTEN; Toward Scalable Cache-Only Memory Architectures; PhD thesis, Royal Institute of Technology, Stockholm; 1992; pps1-262	☐
MB	A32	ASHOK SINGHAL et al.; A High Performance Bus for Large SMPs; In Proceedings of IEEE Hot Interconnects; 1996	☐
MB	A33	M.K. TCHEUN, H. YOON, and S.R. MAENG; An Adaptive Sequential Prefetching Sequential Prefetching Scheme in Shared-Memory Multiprocessors; Department of Computer Science and Technology (KAIST); 1997; pps306-313	☐
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